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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,174	12/05/2003	Frank D. Egitto	END920020086US2 (IEN-10-5	8580

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,174	EGITTO ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-15* is/are rejected.

7)☒ Claim(s) *6,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/5/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 and 2 are objected to because of the following informalities:

Claim 1 recites the limitation "the core" in lines 3, 5, and 7 respectively. The examiner respectfully suggests changing "the core" to --the conductive metal core-- in order to establish proper antecedent basis and consistency throughout the claim language.

Claim 2 recites the limitation "The method according to claim 1 wherein the hole in the deictic layer is prepared by laser drilling, followed by removal of debris, **if any**" in lines 1-2. However, it the recited claim lacks clarity in its meaning and scope because of the term "if any." Appropriate correction is required.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3-5, and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teh et al. (US/6,649,517) in view of Sonderman et al. (US/2002/0192944).

Re claim 1, Teh et al. disclose a method of forming a blind via through a first dielectric layer (11) having a first surface laminated to a conductive metal core (10) (see Fig. 1), the via (13) terminating at a first surface of the conductive metal core (10) (see Fig. 5), comprising the steps of: preparing a contaminant-free hole (13) in the dielectric layer (11) terminating at the surface of the conductive metal core (10) (see Fig. 5), and depositing a conductive metal (not labeled) into the hole (13) to deposit the metal solely on the surface of the conductive metal core and to build the metal deposit from the conductive metal core surface (see Figs. 5-11).

However, Teh et al. do not specifically disclose "plating" process (i.e., the electroless plating process) in order to deposit the conductive metal layer (i.e., copper Cu).

Sonderman et al. disclose electroless plating process in order to deposit copper layer for to dill the via during metallization of the semiconductor device. Sonderman et al. also disclose metalization layer such as copper is difficult to etch and electro-plating process provides depositing of a copper film in the vias with uniform density and with controlled thickness of the deposited copper layer (see Sonderman et al. Pages 1-3).

Both Teh et al. and Sonderman et al. teachings are directed to depositing of copper metallization layer to fill the via hole for copper interconnect. Therefore, the teachings of Teh et al. and Sonderman et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Teh et al. reference with plating process as taught by Sonderman et al. in order to deposit copper layer in the vias with uniform density and controlled thickness.

Re claim 3, as applied to claim 1 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the plated metal is selected from copper (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 4, as applied to claim 3 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the conductive metal is copper that is plated into the hole from the acid copper bath ion using the conductive core as cathode (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 5, as applied to claim 4 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the copper is electroplated in the hole to from a nearly equiaxial fine grained structure (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 7, as applied to claim 1 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the hole is completely filled with metal to form a filled blind via (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 8, as applied to claim 1 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation laminating a second dielectric layer (12 14 16) to a second surface of the first dielectric layer (11), providing a second layer blind via (19) in the second dielectric layer (12 14 16) with the first blind via (13) and having the base of

the second layer via (19) in contact with the first blind via (13) (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 9, as applied to claim 8 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the cross-sectional area of the first layer blind via is larger than the cross-sectional area of the base of the second layer blind via (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 10, as applied to claim 8 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the step of plating a contact pad on the second surface of the first dielectric layer in contact with the filled via (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 11, as applied to claim 1 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein excess metal extending above the dielectric surface is removed to form a landless filled blind via (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 12, as applied to claim 10 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the contact pad has a cross-section that is larger than the cross-section of the base of the second layer blind via (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 13, as applied to claim 1 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the metal is plated in the hole from an electroless plating bath without seeding (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 14, as applied to claim 13 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation laminating a second dielectric layer to the second surface of the first dielectric layer, and providing a second layer blind via aligned with the first blind via and having a base in contact with the contact pad (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

Re claim 15, as applied to claim 13 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations including the limitation wherein the electroless plating bath is a copper bath (see Teh et al. Figs. 5-11 and Sonderman et al. Pages 1-3).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Teh et al. (US/6,649,517) in view of Sonderman et al. (US/2002/0192944), as applied to claim 1 above, and further in view of Hanson (US/5,841,075).

Re claim 2, as applied to claim 13 above, Teh et al. and Sonderman et al. in combination disclose all the claimed limitations. However, both Teh et al. and Sonderman et al. do not specifically disclose forming of the hole in the deictic layer by laser drilling.

Hanson discloses the method of manufacturing a semiconductor device the method includes forming of via holes in the dielectric layer by using laser drilling in order to form blind-vias (see Hanson Col. 3, lines 1-30).

Teh et al., Sonderman et al. and Hanson teachings are directed to depositing of copper metallization layer to fill the via hole for copper interconnect. Therefore, the teachings of Teh et al., Sonderman et al. and Hanson are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Teh et al. and Sonderman et al. with laser drilling as taught by Hanson in order to form blind-vias in the dielectric layer.

Allowable Subject Matter

5. Claims 6, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Yu et al. (US/6,287,768) also disclose similar inventive subject matter.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
November 14, 2004